REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Office Action dated September 9, 2004. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 1-3, 6, 7, 13, 17, 20-22, 30, 31, 33-37, 39 and 41-45 are pending in this application. Claims 4, 6 and 14 are being cancelled without prejudice or disclaimer. Claims 1-3, 6, 7, 13, 17, 20-22, 30, 31, 33-37 and 39 are being amended, as set forth in the above marked-up presentation of the claim amendments, in order to more particularly define and distinctly claim applicants' invention. New claims 41-45 are being added to recited other embodiments of the elected species described in the specification. Applicant hereby submits that no new matter is being introduced into the application through the submission of this response.

Formality Rejection

Figure 20 was objected to because the figure was not labeled as "Prior Art" and the Examiner has requested correction thereof. As indicated, the drawing is being amended as suggested or required by the Examiner. Accordingly, the withdrawal of the outstanding informality rejections is in order, and is therefore respectfully solicited.

Prior Art Rejections

Claims 1-4, 6-7, 13-14, 17, 20-22, 30-31, 33-37 and 39 were rejected under 35 U.S.C. § 102(e) on the grounds of being anticipated by US Patent No. 6,274,895 to Fujii et al. (hereinafter "Fujii"). The prior art references of Kikushima et al. (5,514,895), Ito (5,946,477), Chu et al. (6,714,903) and Suzuki et al. (6,622,293) were cited as being pertinent to the present application. These rejections have been carefully considered, but are most respectfully traversed.

The semiconductor device of the invention (e.g., Fig. 2), as now recited in claim 1, comprises a plurality of signal terminals Ts of a circuit block MC1 ("*This terminal Ts is a*

IN THE DRAWINGS:

Please enter the attached corrected drawing Fig. 20, in which a legend "Prior Art" is being added, to replace Fig. 20 as originally filed. A Letter to Draftsperson is also submitted herewith.

conductor unit for sending and receiving a signal between a circuit formed in the macro cell MC1 and a circuit outside the macro cell MC1 and formed using wiring on the top wiring layer in the MC cell MC 1" p. 10, last paragraph). The signal terminals Ts are arranged within a frame of the circuit block MC1 ("*arranging the terminal Ts in the cell frame*" p. 12, line 2) and along a second direction Y that intersects a first direction X along which a plurality of wirings L extend. The wirings L are wirings of an upper layer and outside the circuit block MC1 (i.e., outside-cell wirings as defined on p. 7, 3rd paragraph), and the wirings L are connected to the signal terminals Ts via a plurality of through holes THs ("*The outside-cell wiring L is electrically connected to the terminal Ts via a through hole TH*" p. 13, lines 3-4). Each of the signal terminals Ts extends in the second direction Y so that a dimension thereof in the second direction Y passes through at least two of the plurality of wirings L ("*the terminal Ts extends to the direction of Y axis and is formed so that the plural wiring lattice lines that extend to the direction of X axis can pass through it.*" p. 12, lines 15-18).

The invention is also directed to a semiconductor device (Fig. 3), as recited in claim 13, comprising: a plurality of circuit blocks recited in claim 1 and arranged along a first direction. Claim 33 recited a semiconductor device as in claim 13 and specifies the circuit blocks as memory circuits.

The circuit block MC1 is defined on page 6, 3rd paragraph, which can be a RAM, a ROM, a PLA, a multiplier, an adder or a data path, a CPU or an analog cell and an I/O (input/output) cell. T "*The area of the macro cell MC 1 can be reduced by arranging the terminal Ts within the cell frame in this manner (that is, using an inner terminal). Further, the plural terminals Ts can be arranged without increasing the area of the macro cell MC 1* (p. 12, lines 1-4)." "*The plural macro cells MC 1 can be arranged without any gap (even if a wiring area is not provided between the cells) by using the structure of such macro cell MC 1* (p. 13, lines 8-11)." In contrast, the prior art (e.g., Fig. 20) requires wiring areas 54 between circuit block 52 for placing outside-cell wirings 53a, 53b thereby transmitting signals between the circuit block 52 (p. 2, 1st paragraph).

Applicants respectfully contend that none of the cited prior art reference teaches or suggest a semiconductor device with "such signal terminals Ts arranged along a second direction Y and each extending in the second direction Y so that a dimension thereof in the second direction Y passes through at least two of the plurality of outside-cell wirings L" as the invention.

In contrast, Fujii's interconnections M1, M2, M3 are outside-cell wirings (Fig. 8),

rather than any signal terminals Ts are arranged within a frame of the circuit block. In addition, although Fujii's slit cells are in-cell wirings in dedicated areas and used when the number of the interconnections for transferring the input signal to the cells is insufficient (col. 6, line 41-56; Fig. 3), each of the slit cells extends along the same/first direction as the interconnections M1, M2, rather than extending in a second direction crossing the first direction so that a dimension thereof in the second direction passes through at least two of the plurality of outside-cell wirings M1, M2. As the slit cells and the interconnections M1, M2 are arranged in parallel (Fig. 3), none of the slit cells will passes through at least two of the plurality of outside-cell wirings M1, M2. As such, Fujii shares the same deficiencies, i.e., requiring wiring areas for connecting between circuit blocks which results in a wasteful area on a semiconductor chip thereby increasing a chip size, as the prior art described on page 1, line 23 to page 2, line 9 as well as shown in Fig. 20 of the specification.

Applicants contend that neither Fujii, nor other cited references teaches or discloses each and every feature of the present invention as disclosed in independent claims 1, 13 and 33. As such, the present invention as now claimed is distinguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

Conclusion

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference upon which the rejections in the Office Action rely, Applicants respectfully contend that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicants' undersigned representative at the address and phone number indicated below.

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